

ChengXiang Qi

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Education

University of Chinese Academy of Sciences

Master of Computer Architecture

2023/08 -

Hangzhou, Zhejiang, China

TianJin University

B. Eng in Computer Science and Technology

2019/09 - 2023/06(Expected)

TianJin, China

- Teaching Assistant for ICS(Introduction to Computer System) in Fall 2021
 - 4.0 Courses: ICS, Computer Architecture, Advanced Computer Architecture, Operating System and so on.
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Skills

- **Programming Languages:** Rust, C, Go, Python, JavaScript, Assembly
 - **Tools:** Linux, Git, GDB, QEMU, Makefile, Docker
 - **System:** Familiar with the concepts and design of operating system kernels, and have experience designing and implementing operating system kernels using the Rust language. Passionate and knowledgeable about the RISC-V instruction set architecture, with multiple projects designed based on the RISC-V instruction set.
 - **Arch:** I have previously designed and implemented a MIPS 32-bit processor core, have read some of CAAQA, and have implemented a out-of-order simulator of tomasulo algorithm in Rust.
 - **Storage/DB:** Self-taught CMU 15-445, TiKV talent-plan, and some of MIT 6.824 and completed the corresponding labs.
 - **Open Source Contributions:** I have contributed code to multiple open source projects such as @rCore-Tutorial-v3, @cs-self-learning, and @rustyvisor, and my personal open source projects have a total of over 400 stars.
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Selected Awards

- NSCSCC Team Competition Third Prize in 2022
 - OSCOMP Team Competition Thrid Prize in 2021
 - Summer OSPP The Best Quality Award in 2021
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Selected Projects

ko-ok-OS/xv6-rust(★169)

2021/02 - 2021/08

- A Unix-like operating system implemented pure rust.
- Optimize memory module using Buddy Sytem.
- Redesign Spinlock/Sleeplock as smart pointer.
- Optimize file system, making it support Rust features.

hypocaust-2(★17)

2023/02 - Now

- A hardware-assisted RISC-V type-1 hypervisor written in Rust.
- Implement SBI call process, two stage page table translation, PLIC emulation(interrupt inject), exception delegation, passthrough or emulate devices.
- Capable of booting rCore-Tutorial-v3, RT-Thread, Linux mainline.

hypocaust(★29)

2023/01 - 2023/02

- A S mode trap & emulate RISC-V type-1 hypervisor written in Rust.
- Implement SBI call process, shadow page table construction, synchronization between shadow page table and guest page table, PLIC emulation(interrupt inject), exception delegation, passthrough or emulate devices.
- Capable of booting minikernel(a small os kernel with filesystem).

rCore-fat

2021/07 - 2021/08

- Design fat32 file system for rCore-Tutorial-v3, it is a alternative topic of rCore OS community in Summer OSPP 2021.
 - It can run successfully on qemu and k210 development boards.
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Talks & Presentations

Hypocaust, a Type-1 RISC-V hypervisor

2023/03/26

Invited talk in OS2ATC 2022

Beijing, China

- slide: <http://kuangjux.top/file/talks/hypocaust.pdf>

- vedio: <https://live.csdn.net/room/csdnlive5/VKfSCOiR>
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Experience

Summer OSPP 2021

2021/07 - 2021/09

- Participated in the work of the rcore-os community and supported the FAT32 file system for rCore-Tutorial-v3, successfully running it on QEMU and K210. My work won the Best Quality Award for the Summer of Open Source in 2021.

TWT Studio

2019/09 - 2021/02

Software Engineer

TianJin, China

- Developed a management system for the school management system in Vue.js and it can run stably on the server.
- Maintained the school's party building system in PHP and participated in part of the system's reconstruction work.